ESD Association Standard

ANSI/ESD S5.3.1-2009

ANSI/ESD S5.3.1-2009

Revision and Redesignation of ANSI/ESD STM5.3.1-1999

For Electrostatic Discharge Sensitivity Testing –

Charged Device Model (CDM) – Component Level

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440

An American National Standard
Approved December 4, 2009

ESD Association Standard for Electrostatic Discharge Sensitivity Testing –

Charged Device Model (CDM) – Component Level

Approved July 31, 2009
ESD Association

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FOREWORD

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a component and discharging through the component. However, with the increasing use of automated component handling systems another potentially destructive discharge mechanism, the charged device model (CDM) becomes increasingly important. In the CDM a component itself becomes charged (e.g., by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object.

Accurately quantifying the CDM discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the component will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS components for the CDM model is dielectric damage, although other damage has been noted.

The CDM sensitivity of a given component is package dependent. An integrated circuit (IC) chip in a small outline package (SOP) configuration may be more susceptible to CDM damage when compared to a dual-in-line (DIL) package configuration. ICs in thin, small outline packages (TSOP), or pin grid array (PGA) packages typically have the lowest CDM withstand voltage.

Based on results obtained with early CDM testers (not necessarily meeting the waveform requirements of this standard), components with CDM sensitivities of 500 volts or less proved difficult to handle without damage. Components with CDM sensitivities of 1,000 volts or more did not experience major field problems when proper handling techniques were followed. Recent data indicate with proper ESD controls, safe handling of devices with CDM sensitivities of 250V is achieved.

Waveform parameters for the 30 pF verification module may be subject to change in future revisions of this document.

This CDM document does not apply to the socketed discharge model testers.

This document was originally designated ANSI/ESD STM5.3.1-1999 and approved on September 26, 1999. This standard[1] is a revision of ANSI/ESD STM5.3.1-1999 and was approved on July 31, 2009. This standard was prepared by the 5.3.1 (CDM) Device Testing Subcommittee.

[1] ESD Association Standard (S): A precise statement of a set of requirements to be satisfied by a material, product, system or process that also specifies the procedures for determining whether each of the requirements is satisfied.

At the time ANSI/ESD S5.3.1-2009 was prepared, the 5.3.1 (CDM) Device Testing Subcommittee had the following members:

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