ESD Association Standard Practice

For the Protection of Electrostatic Discharge Susceptible Items

Electrostatic Discharge Sensitivity Testing – Very Fast Transmission Line Pulse (VF-TLP) – Component Level

ANSI/ESD SP5.5.2-2007

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
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Approved September 16, 2007
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FOREWORD

This standard practice defines a method for pulse testing to evaluate the voltage current response of the component under test. This technique is known as “transmission line pulse” (TLP) testing.

Interest in very fast transmission line pulse (VF-TLP) testing is growing rapidly in the testing of electronic components in the semiconductor industry. VF-TLP testing techniques are being used for semiconductor process development, device and circuit design. This technique or practice is being utilized on products in both wafer level and packaged environments. VF-TLP testing is used as an ESD characterization tool to obtain voltage-current pulse characterization parameters, failure levels, and ESD metrics. The VF-TLP technique is being used today as a standard measurement for ESD devices. The VF-TLP system to the ESD engineer is becoming a tool as critical as the “parameter analyzer” is to the semiconductor engineer.

Today there is no industrial standard or specification to best describe VF-TLP testing. This document is intended to serve as an interim step toward establishment of a VF-TLP specification for the industry. Today, the majority of systems are designed by engineers in a laboratory environment. As of this writing, a number of commercial VF-TLP systems have been marketed in the industry. Hence it is clear a VF-TLP specification is needed for the TLP vendors, semiconductor industry and product customers to be able to make valid data comparisons. With the usage of VF-TLP data for ESD characterization, technology benchmarking, and product quality evaluation, there is a growing need to have standard methodologies, failure criteria, and means of reporting to allow dialogue between semiconductor suppliers, vendors, and product customers.

This document defines the standard practice used today in the semiconductor industry for VF-TLP testing method and techniques in both industrial and academic institutions. (This document is intended to be used by electrical technicians, electrical engineers, semiconductor process and device engineers, ESD reliability and quality engineers, and circuit designers.) The document is to act as an educational guide, a learning document, and as a reference for the practices being used today. The values stated in the document are guidelines, not specifications. The values stated are the majority consensus of the contributors from both industry and academic environments.

The context of this document is the application of VF-TLP techniques for the electrical characterization of semiconductor components. These semiconductor components can be single devices, a plurality of devices, integrated circuits, or semiconductor chips. This methodology is relevant to both active and passive elements. This test method is applicable to diodes, MOSFET devices, bipolar transistors, resistors, capacitors, inductors, contacts, vias, wire interconnects and related components.

This standard practice was processed and approved for submittal to the ESD Association Standards Committee by the 5.5 Device Testing (TLP) Subcommittee in 2006. At that time, the 5.5 Device Testing (TLP) Subcommittee had the following members:

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1.0 SCOPE AND PURPOSE

1.1 Scope

The scope and focus of this document pertains to very fast transmission line pulse (VF-TLP) testing techniques of semiconductor components.

1.2 Purpose

The purpose of the document is to establish guidelines and standard practices presently used by development, research, and reliability engineers in both universities and industry for VF-TLP testing. This document explains a methodology for both testing and reporting information associated with VF-TLP testing.

2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0, ESD Association's Glossary of Terms[1]

ANSI/ESD STM5.1, Human Body Model (HBM) – Component Level[1]

ESD DS5.2, Machine Model (MM) – Component Level[1]

ESD DS5.3.1, Charged Device Model (CDM) – Component Level[1]

ANSI/ESD SP5.5.1, Transmission Line Pulse (TLP) Component Level[1]

3.0 DEFINITIONS

The following definitions are in addition to those found in ESD ADV 1.0, ESD Association's Glossary of Terms:

Very Fast Transmission Line Pulse (VF-TLP). A rectangular current pulse formed by discharging a charged transmission line cable. In this document, VF-TLP refers to any rectangular pulse formed from any pulse source with a fast rise time and short pulse width.

Very Fast Transmission Line Pulse Test System. A test system that applies a rectangular pulse to a device under test and allows measurement of device electrical characteristics during a pulsed state. The system typically measures current and voltage across the device, as well as leakage current after VF-TLP pulse application.

4.0 SAFETY

4.1 Personnel Safety

The procedures and equipment described in this document may expose personnel to hazardous electrical conditions. Users of this document are responsible for selecting equipment that complies with applicable laws, regulatory codes and external and internal policy. Users are cautioned that this document cannot replace or supersede any requirements for personnel safety.

Ground Fault Circuit Interrupters (GFCI) and other safety protection should be considered wherever personnel might come in contact with electrical sources.

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