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ESD Association Standard Practice

ANSI/ESD SP5.0-2018

For Electrostatic Discharge Sensitivity Testing

Reporting ESD Withstand Levels on Datasheets

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440

An American National Standard
Approved February 22, 2019

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ESD Association Standard Practice for Electrostatic Discharge Sensitivity Testing –

Reporting ESD Withstand Levels on Datasheets

Approved September 17, 2018
EOS/ESD Association, Inc.

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Published by:

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440

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Printed in the United States of America

ISBN: 1-58537-308-7

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(This foreword is not part of ESD Association Standard Practice ANSI/ESD SP5.0-2018)

FOREWORD

This standard practice[1] provides a standardized approach and template for the inclusion of device-level ESD withstand levels in datasheets or other similar product information documentation. This work was initiated to solve a long-standing problem with communication of such data to users of devices. At the time of the release of this document, a survey of device datasheets found many were missing any ESD information. Provided information was often incomplete. For example, often only human body model (HBM) levels were included and charged device model (CDM) levels were missing; even though CDM is widely regarded as the more significant cause of ESD failures in a production environment. The goal is that the use of this standardized approach will improve the communication of complete ESD information (HBM and CDM).

The template also provides guidelines for elaborating on the ESD performance of the device. The template is particularly useful when a supplier wants to convey information that gives additional information about relative ESD risk, identification of the most sensitive pins or discussion of performance relative to ESD targets of a given device family or technology. Finally, the template includes language which clarifies that HBM and CDM withstand threshold are relevant only to handling in an ESD protected area (EPA) and that these ratings do not predict, and are not relevant to, performance in system-level tests.

This document was designated ANSI/ESD SP5.0-2018 and approved on September 17, 2018.

At the time ANSI/ESD SP5.0-2018 was prepared, the 5.0 Device Testing subcommittee had the following members:

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Wolfgang Stadler Intel Deutschland GmbH		Scott Ward Texas Instruments

[1] **ESD Association Standard Practice:** A procedure for performing one or more operations or functions that may or may not yield a test result. Note, if a test result is obtained it may not be reproducible.

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ESD Association Standard Practice for Electrostatic Discharge Sensitivity Testing – Reporting ESD Withstand Levels on Datasheets

1.0 PURPOSE

This document is intended to guide device manufacturers in developing datasheets and to device customers in understanding datasheet entries. Standardized ESD stress test methods have been developed to evaluate the relative sensitivity of devices. Although these methods are available, the results of the testing are not always provided by the suppliers, especially charged device model (CDM) levels. The document provides a standardized template which includes a minimum information set and gives guidelines for expanded individual pin information when needed. The document should improve the availability and usefulness of reported ESD data.

2.0 SCOPE

This document applies to ESD withstand level information in datasheets or other information publications such as reliability or qualification reports. All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, optoelectronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) should have this information provided.

NOTE: This document does not apply to electrically-initiated explosive devices, flammable liquids, or powders.

3.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision or amendment form a part of this document to the extent specified herein:

ANSI/ESDA/JEDEC JS-001, Human Body Model (HBM) – Component Level[2,3]

ANSI/ESDA/JEDEC JS-002, Charged Device Model (CDM) – Device Level[2,3]

ESD ADV1.0, Glossary of Terms[2]

IEC 61000-4-2, Testing and Measurement Techniques – Electrostatic Discharge Immunity Test[4]

JEDEC JESD47, Stress-Test Driven Qualification of Integrated Circuits[3]

4.0 DEFINITIONS

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, EOS/ESD Association, Inc.'s Glossary of Terms available for complimentary download at www.esda.org.

ESD withstand level. The highest voltage level that does not cause device failure; the device passes all tested lower voltage levels.

5.0 GENERAL CONSIDERATIONS

There are several important points to consider when using this document, either to develop datasheets or in reading datasheets.

- The standard test methods used, including version, should be cited. In most cases, these will be ANSI/ESDA/JEDEC JS-001-20xx (HBM) and ANSI/ESDA/JEDEC JS-002-20yy (CDM). Other standards from accredited standards bodies may also be used.
- Complete ESD handling characterization of devices requires BOTH HBM and CDM as specified in JEDEC JESD 47.

[2] EOS/ESD Association, Inc., 7900 Turin Road, Bldg. 3, Rome, NY 13440; Ph: 315-339-6937; www.esda.org
[3] JEDEC, 3103 North 10th Street, Arlington, VA 22201; Ph: 703-907-7534; www.jedec.org
[4] IEC – International Electrotechnical Commission, www.iec.ch