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FOREWORD

This document defines a method for pulse testing to evaluate the voltage-current response of the component under test. This technique is known as transmission line pulse (TLP) testing. Interest in TLP testing is growing rapidly in the testing of electronic components in the semiconductor industry. TLP testing techniques are being used for semiconductor process development, device and circuit design. This technique or practice is being utilized on products in both wafer level and packaged environments. TLP testing is used as an ESD characterization tool to obtain voltage-current pulse characterization parameters, failure levels, and ESD metrics. The TLP technique is being used today as a standard measurement for ESD devices. The TLP system to the ESD engineer is becoming a tool as critical as the “parameter analyzer” is to the semiconductor engineer.

The majority of TLP systems are designed by engineers in a laboratory environment. A number of commercial TLP systems have been marketed in the industry. Hence, it is clear a TLP specification was needed for the TLP vendors, semiconductor industry and product customers to be able to make valid data comparisons. With the usage of TLP data for ESD characterization, technology benchmarking, and product quality evaluation, there is a growing need to have standard methodologies, failure criteria, and means of reporting to allow dialogue between semiconductor suppliers, vendors, and product customers.

This document defines the standard test method used today in the semiconductor industry for TLP testing method and techniques in both industrial and academic institutions. (This document is intended to be used by electrical technicians, electrical engineers, semiconductor process and device engineers, ESD reliability and quality engineers, and circuit designers.) This document covers standard TLP (pulse width in the order of 100 ns). Other TLP variants may be covered in other documents.

The context of this document is the application of TLP techniques for the electrical characterization of semiconductor components. These semiconductor components can be single devices, a plurality of devices, integrated circuits, or semiconductor chips. This methodology is relevant to both active and passive elements. This test method is applicable to diodes, MOSFET devices, bipolar transistors, resistors, capacitors, inductors, contacts, vias, wire interconnects, and related components.

This document was originally designated ANSI/ESD SP5.5.1-2004, and approved on February 22, 2004. ANSI/ESD STM5.5.1-2008 was a revision and re-designation of ANSI/ESD SP5.5.1-2004 and was approved on February 24, 2008. ANSI/ESD STM5.5.1-2014 is a revision of ANSI/ESD STM5.5.1-2008 and was approved on August 26, 2014.

---

1 ESD Association Standard Test Method (STM): A definitive procedure for the identification, measurement and evaluation of one or more qualities, characteristics, or properties of a material, product, system, or process that yield a reproducible test results.
At the time ANSI/ESD STM5.5.1-2014 was prepared, the 5.5 (TLP) Device Testing Subcommittee had the following members:

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# TABLE OF CONTENTS

1.0 PURPOSE AND SCOPE ........................................................................................................... 1
  1.1 PURPOSE ......................................................................................................................... 1
  1.2 SCOPE ............................................................................................................................. 1

2.0 REFERENCED PUBLICATIONS .......................................................................................... 1

3.0 DEFINITIONS ....................................................................................................................... 1

4.0 PERSONNEL SAFETY ........................................................................................................... 3

5.0 EQUIPMENT .......................................................................................................................... 3
  5.1 OSCILLOSCOPE ............................................................................................................... 3
  5.2 VOLTAGE PROBE ......................................................................................................... 3
  5.3 CURRENT PROBE .......................................................................................................... 3
  5.4 TRANSMISSION LINE .................................................................................................... 3
  5.5 HIGH VOLTAGE POWER SUPPLY .................................................................................. 4
  5.6 HIGH VOLTAGE SWITCH ............................................................................................... 4
  5.7 ATTENUATOR .................................................................................................................... 4
  5.8 RISE TIME FILTER ......................................................................................................... 4

6.0 TLP WAVEFORM PARAMETERS ......................................................................................... 5
  6.1 PULSE WIDTH ................................................................................................................ 5
  6.2 RISE TIME .................................................................................................................... 5
  6.3 FALL TIME ................................................................................................................... 5
  6.4 PEAK CURRENT OVERSHOOT ...................................................................................... 5
  6.5 CURRENT RINGING DURATION ...................................................................................... 5
  6.6 PEAK VOLTAGE OVERSHOOT ....................................................................................... 5
  6.7 VOLTAGE RINGING DURATION ..................................................................................... 5
  6.8 MEASUREMENT WINDOW ............................................................................................... 5

7.0 TEST REQUIREMENTS AND PROCEDURES ................................................................. 7
  7.1 ERROR CORRECTION AND CALIBRATION .................................................................. 7
  7.2 TESTER ERROR CORRECTION METHODOLOGY ......................................................... 7
    7.2.1 Short Circuit Error Correction Methodology ............................................................ 7
    7.2.2 Open Circuit Error Correction Methodology ......................................................... 7
  7.3 TESTER CALIBRATION METHODOLOGY .................................................................... 7
    7.3.1 Voltage Calibration Methodology .............................................................................. 8
    7.3.2 Current Calibration Methodology ............................................................................ 8
  7.4 TLP TEST PROCEDURE .................................................................................................. 8
ANNEXES

Annex A (Informative): TLP Design Guidelines .............................................................. 11
Annex B (Informative): Evaluation and Determination of Failure ................................. 18
Annex C (Informative): Verification Failures .................................................................. 20
Annex D (Informative): Revision History for ANSI/ESD STM5.5.1-2014 ....................... 21

TABLES

Table 1: TLP Current and Voltage Pulse Parameters ..................................................... 4
Table 2: TLP Methodologies and Parameters ................................................................. 12

FIGURES

Figure 1: Typical TLP Plot Illustrating Several Parameters that can be Obtained from this Measurement ........................................................................................................ 2
Figure 2: TLP Waveform Parameter Illustration for Pulse Width Rise Time and Fall Time .......................................................... 6
Figure 3: Illustration of Peak Current Overshoot .............................................................. 6
Figure 4: Illustration of Peak Voltage Overshoot .............................................................. 6
Figure 5: Flow Diagram for the TLP Component Test Procedure ..................................... 9
Figure 6: Illustration of TLP Pulse Sequence .................................................................. 10
Figure 7: Current Source TLP ........................................................................................ 13
Figure 8: Time Domain Reflectometer (TDR) TLP .......................................................... 13
Figure 9: Time Domain Transmission (TDT) TLP ............................................................ 14
Figure 10: Time Domain Reflection and Transmission (TDRT) TLP .................................. 14
Figure 11: Kelvin Set-up ................................................................................................. 17
1.0 PURPOSE AND SCOPE

1.1 Purpose
The purpose of the document is to establish a methodology for both testing and reporting information associated with transmission line pulse (TLP) testing.

1.2 Scope
The scope and focus of this document pertains to TLP testing techniques of semiconductor components.

2.0 REFERENCED PUBLICATIONS
Unless otherwise specified, the following documents of the latest issue, revision or amendment, form a part of this standard to the extent specified herein:
- ESD ADV1.0, ESD Association Glossary of Terms
- ANSI/ESDA/JEDEC JS-001 – Human Body Model (HBM)
- ANSI/ESD S5.3.1 – Charged Device Model (CDM)

3.0 DEFINITIONS
The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association’s Glossary of Terms available for complimentary download at www.esda.org.
The terms defined in this section are specific to this document. Figure 1 illustrates these terms pictorially on a TLP I-V plot and leakage plot.
NOTE: These definitions may not be applicable to all devices.

- **V<sub>A</sub>:** avalanche voltage or breakdown voltage. Voltage at which current through a reverse biased junction starts to increase significantly due to avalanche multiplication.
  NOTE: This does not apply to non-snapback devices – see Turn-on Voltage for diode stack clamps.

- **V<sub>t1</sub>, I<sub>t1</sub>:** trigger point. The voltage/current at which bipolar action starts in a snapback device.

- **V<sub>hold</sub>, I<sub>hold</sub>:** holding point. The voltage at the apparent lowest current after snapback. This point depends on the Device Under Test (DUT) and the source impedance of the measurement setup.

- **V<sub>on</sub>:** turn-on voltage. The point at which the linear fit through the linear part of the TLP I-V curve after the holding point crosses the voltage axis.

- **R<sub>on</sub>:** on-state resistance. The equivalent resistance of the slope (conductance G<sub>on</sub>) of the linear fit through the linear part of the TLP I-V curve after the holding point.

- **V<sub>clamp</sub>:** clamping voltage. DUT voltage at a given ESD current (I<sub>ESD</sub>), in approximation:
  \[ V_{\text{clamp}} = V_{\text{on}} + R_{\text{on}} \times I_{\text{ESD}}. \]

- **V<sub>t2</sub>, I<sub>t2</sub>:** 2<sup>nd</sup> breakdown point. The voltage/current at which the DUT characteristic shows a (second) snapback. This second snapback can also be the point at which the device shows destructive damage, typically seen as a large change in the evaluation measurement (often

2 ESD Association, 7900 Turin Road, Bldg. 3, Rome, NY 13440, Ph: 315-339-6937; FAX: 315-339-6793; www.esda.org