This is a preview of "ESD TR5.5-03-14". Click here to purchase the full version from the ANSI store.

ESD Association Technical Report

ESD TR5.5-03-14

For Electrostatic Discharge Sensitivity Testing –

Very-Fast Transmission Line Pulse (VF-TLP) – Round Robin Analysis

Authors:

Working Group 5.5, Transmission Line Pulse

ESD Association

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440

This is a preview of "ESD TR5.5-03-14". Click here to purchase the full version from the ANSI store.

CAUTION NOTICE

Electrostatic Discharge Association (ESDA) standards and publications are designed to serve the public interest by eliminating misunderstandings between manufacturers and purchasers, facilitating the interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining the proper product for his particular needs. The existence of such standards and publications shall not in any respect preclude any member or non-member of the Association from manufacturing or selling products not conforming to such standards and publications. Nor shall the fact that a standard or publication that is published by the Association preclude its voluntary use by non-members of the Association, whether the document is to be used either domestically or internationally. Recommended standards and publications are adopted by the ESDA in accordance with the ANSI Patent policy.

Interpretation of ESDA Standards: The interpretation of standards in-so-far as it may relate to a specific product or manufacturer is a proper matter for the individual company concerned and cannot be undertaken by any person acting for the ESDA. The ESDA Standards Chairman may make comments limited to an explanation or clarification of the technical language or provisions in a standard, but not related to its application to specific products and manufacturers. No other person is authorized to comment on behalf of the ESDA on any ESDA Standard.

DISCLAIMER OF WARRANTIES

THE CONTENTS OF ESDA'S STANDARDS AND PUBLICATIONS ARE PROVIDED "AS-IS," AND ESDA MAKES NO REPRESENTATIONS OR WARRANTIES, EXPRESSED OR IMPLIED, OF ANY KIND, WITH RESPECT TO SUCH CONTENTS. ESDA DISCLAIMS ALL REPRESENTATIONS AND WARRANTIES, INCLUDING WITHOUT LIMITATION, WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR USE, TITLE, AND NON-INFRINGEMENT.

DISCLAIMER OF GUARANTY

ESDA STANDARDS AND PUBLICATIONS ARE CONSIDERED TECHNICALLY SOUND AT THE TIME THEY ARE APPROVED FOR PUBLICATION. THEY ARE NOT A SUBSTITUTE FOR A PRODUCT SELLERS' OR USERS' OWN JUDGEMENT WITH RESPECT TO ANY PARTICULAR PRODUCT DISCUSSED, AND ESDA DOES NOT UNDERTAKE TO GUARANTEE THE PERFORMANCE OF ANY INDIVIDUAL MANUFACTURERS' PRODUCTS BY VIRTUE OF SUCH STANDARDS OR PUBLICATIONS. THUS, ESDA EXPRESSLY DISCLAIMS ANY RESPONSIBILITY FOR DAMAGES ARISING FROM THE USE, APPLICATION, OR RELIANCE BY OTHERS ON THE INFORMATION CONTAINED IN THESE STANDARDS OR PUBLICATIONS.

LIMITATION ON ESDA's LIABILITY

NEITHER ESDA, NOR ITS MEMBERS, OFFICERS, EMPLOYEES OR OTHER REPRESENTATIVES WILL BE LIABLE FOR DAMAGES ARISING OUT OF, OR IN CONNECTION WITH, THE USE OR MISUSE OF ESDA STANDARDS OR PUBLICATIONS, EVEN IF ADVISED OF THE POSSIBILITY THEREOF. THIS IS A COMPREHENSIVE LIMITATION OF LIABILITY THAT APPLIES TO ALL DAMAGES OF ANY KIND, INCLUDING, WITHOUT LIMITATION, LOSS OF DATA, INCOME OR PROFIT, LOSS OF OR DAMAGE TO PROPERTY, AND CLAIMS OF THIRD PARTIES.

Published by:

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440

Copyright © 2014 by ESD Association
All rights reserved

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

Printed in the United States of America

This is a preview of "ESD TR5.5-03-14". Click here to purchase the full version from the ANSI store.

(This foreword is not part of ESD Association Technical Report ESD TR5.5-03-14)

FOREWORD

The ESD Association's working group 5.5 subcommittee conducted a round robin study to determine if the current VF-TLP standard practice (SP) yielded test results which would allow the elevation of the SP, with suitable modifications to a standard test method (STM). This technical report (TR) covers both the data taken and the analysis methods used to develop a precision statement for VF-TLP. This study involves seven test sites with eleven different test structures evaluated at each site. This paper summarizes these findings.

At the time ESD TR5.5-03-14 was prepared, the 5.5 (TLP) Device Testing Subcommittee had the following members:

Theo Smedes, Chair
NXP Semiconductors

Robert Ashton
ON Semiconductor

Jon Barth
Barth Electronics, Inc.

Lorenzo Cerati
STMicroelectronics

Marcel Dekker
MASER Engineering

Reinhold Gaertner
Infineon Technologies AG

Horst Gieser
Fraunhofer EMFT

Vaughn Gross
Green Mountain ESD Labs, Inc.

Evan Grund
Grund Technical Solutions, LLC

Leo G. Henry
ESDTLP Consultants

Timothy Maloney
Intel Corporation

Thomas Meuse
Thermo Fisher Scientific

Paul Phillips
Phasix ESD

Bill Reynolds
IBM

Alan Righter
Analog Devices

Masanori Sawada
HANWA Electronic Ind. Co., Ltd.

Wolfgang Stadler
Intel Mobile Communications

Steven H. Voldman
Steven H. Voldman LLC

Scott Ward
Texas Instruments

Terry Welsher, TAS Rep
Dangelmayer Associates

This is a preview of "ESD TR5.5-03-14". Click here to purchase the full version from the ANSI store.

The following individuals contributed significantly to the development of ESD TR5.5-03-14:

Detlef Bonfert Fraunhofer EMFT	Aniket Breed Intel	Tilo Brodbeck Infineon
Michael Chaine Micron Technology, Inc.	Charvaka Duvvury ESD Consulting, LLC	Michael Hopkins Hopkins Technical
Justin Katz Grund Technical Solutions, LLC	Mark Kelly Delphi Electronics	Kathleen Muhonen RF Micro Devices
Ravindra Narayan LSI	Nathaniel Peachey RF Micro Devices	Timothy Prass Raytheon
Karen Shrier Electronic Polymers	Larry Ting Texas Instruments	Roger Watkins Grund Technical Solutions, LLC
Heinrich Wolf Fraunhofer EMFT		Eugene Worley Qualcomm

This is a preview of "ESD TR5.5-03-14". Click here to purchase the full version from the ANSI store.

TABLE OF CONTENTS

1.0 INTRODUCTION 1

1.1 TLP BACKGROUND 1
1.2 BRIEF DESCRIPTION OF VF-TLP 2
1.3 VF-TLP ROUND ROBIN BACKGROUND 3

2.0 MEASUREMENTS 4

2.1 ROUND ROBIN GUIDELINES 4
2.2 TEST STRUCTURES 4
2.2.1 Set I: Passive Structures 4
2.2.2 Set I: Active Structures 5
2.2.3 Set II: Structures Shared Between Test Sites 5
2.3 RESULTS 6
2.3.1 Site to Site Comparisons 6
2.3.2 Measurement System Variations 18

3.0 ANALYSIS OF MEASUREMENTS 20

3.1 INTRODUCTION TO ANALYSIS 20
3.2 SAMPLES AND MEASUREMENTS 21
3.3 PRECISION STATEMENT DEVELOPMENT 23
3.3.1 Repeatability 23
3.3.2 Voltage 23
3.3.3 Resistance 24
3.3.4 Current 24
3.4 PRECISION STATEMENT 25

4.0 CONCLUSIONS AND OUTLOOK 25

4.1 CONCLUSIONS ON RAW DATA AND CONDUCTING OF THE RR 25
4.1.1 Handling of Oscilloscope Range Changing 25
4.1.2 Measurement Windows 25
4.1.3 Sensitivity of Snapback Devices 25
4.1.4 Current Reference Standard 26
4.1.5 RF Versus 50-ohm Needle Probes 26
4.1.6 Excessive Measurement Noise 26
4.2 CONCLUSIONS ON THE PRECISION STATEMENT 26
4.3 OUTLOOK FOR VF-TLP 26

5.0 BIBLIOGRAPHY 26

This is a preview of "ESD TR5.5-03-14". Click here to purchase the full version from the ANSI store.

TABLES

Table 1: Extracted Parameters per Test Structure from I-V Data at 5 ns Pulse Width, Set I......... 7
Table 2: Extracted Parameters per Test Structure from I-V Data at 1.25 ns Pulse Width, Set I ... 7
Table 3: Extracted Parameters per Test Structure from I-V Data at 1.25 ns Pulse Width, Set II Passive........ 8
Table 4: Extracted Parameters Per Test Structure from I-V Data at 1.25 ns Pulse Width, Set II Zener Diodes 8
Table 5: Extracted Parameters per Test Structure from I-V Data at 1.25 ns Pulse Width, Set II Transistors 8
Table 6: Samples and Measured Parameters in the RR Studies........ 21
Table 7: Details of Samples Used in Statistical Analysis 21
Table 8: Summary of Voltage Measurements and Standard Deviations 23
Table 9: Summary of Voltage Measurements and R Values 23
Table 10: R% Values for Voltage 24
Table 11: Summary of Resistance Measurements and R Values........ 24
Table 12: R% Values for Resistance........ 24
Table 13: R% Values for Voltage and Resistance as well as Values for Current Calculated using Linear and Quadratic Addition 25
Table 14: Expected Precision of VF-TLP Measurements for Voltage and Current........ 25

FIGURES

Figure 1 Time Domain Reflection (TDR) TLP system 2
Figure 2: Time Domain Reflection and Transmission VF-TLP System........ 3
Figure 3: Time Domain Transmission VF-TLP System........ 3
Figure 4: Open, Short, 5 ohm and 50 Ohm Test Structures 5
Figure 5: Diode Stack and Snapback Structures 5
Figure 6: 5-Ohm Structure........ 9
Figure 7: 50-Ohm Structure........ 10
Figure 8: Diode Stack 11
Figure 9: Diode Stack Turn on Voltage, Vt1 12
Figure 10: Illustration of Holding Voltage for the Snapback 13
Figure 11: Snapback Measured at 5 ns and 1.25 ns Pulse Width 14
Figure 12: Snapback Voltage, Vsb 14
Figure 13: 5 ohm Resistors, A and B, Set II 15
Figure 14 : Zener Diode A, Set II........ 16
Figure 15: Zener Diode B, Set II........ 16
Figure 16: Zener Diode C, Set II........ 17
Figure 17: JFET Transistor 310, Set II 17
Figure 18: JFET Transistor 545C, Set II........ 18
Figure 19: Snapback Measured with a 4 GHz and a 6 GHz Scope 18
Figure 20: Snapback I-V Plots for 1.25 ns and 5 ns Pulses........ 19
Figure 21: Diode Stack, 1.25 ns, RF, and Needle Probes 20
Figure 22: Snapback, 5 ns, RF and Needle Probes........ 20