



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-4761

Design Guide for Protection of Printed Board Via Structures

Developed by the Via Protection Task Group (D-33d)
of the Rigid Printed Board Committee (D-30) of IPC

Users of this publication are encouraged to participate in the
development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1219
Tel 847 615.7100
Fax 847 615.7105

Table of Contents

1 SCOPE	1
1.1 Purpose	1
1.2 Terms and Definitions	1
2 APPLICABLE DOCUMENTS	1
2.1 IPC	1
3 PWB FABRICATION AND ASSEMBLY GUIDELINES	2
3.1 Advantages of Via Protection	2
3.2 PWB Fabrication Issues	2
3.2.1 Fill or Plug Separation from Plated Hole Wall	3
3.2.2 Voids	3
3.3 Assembly Process Issues	3
3.4 Long Term Reliability Concerns	4
4 MATERIALS/DESIGN CONSIDERATIONS	4
4.1 End Use Considerations	4
4.2 Fabrication Considerations	5
4.3 Assembly Considerations	5
4.4 Types of Materials for Filled/Plugged	5
4.4.1 Non-conductive (Organic) – Non-imageable ..	5
4.4.2 Non-conductive – Photoimageable	5
4.4.3 Conductive Ink	5
4.5 Materials for Tented/Covered Via Structures ..	5
4.5.1 Tented Only	5
4.5.2 Tented and Covered	5
4.6 Material Specification and Selection	6
5 VIA PROTECTION DEFINITIONS AND TYPES ...	6
5.1 Tented Via (Type I Via)	6
5.2 Tented and Covered Via (Type II Via)	7
5.3 Plugged Via (Type III Via)	8
5.4 Plugged and Covered Via (Type IV Via)	8
5.5 Filled Via (Type V Via)	9
5.6 Filled and Covered Via (Type VI Via)	9
5.7 Filled and Capped Via (Type VII Via)	9
5.8 Partially Filled Via	10
6 PERFORMANCE TRADEOFFS	10
6.1 Planarity	10
6.2 Via Metallization	10

6.3 Moisture Absorption	11
6.4 Cleanliness Concerns	11
6.5 Use of Conformal Coating	11
7 SAMPLE DESIGNS	11
8 EXAMPLES OF DRAWING NOTES	12

Figures

Figure 1-1 Bumped Via Protection Material	1
Figure 1-2 Dimpled Via Protection Material	1
Figure 1-3 Planarized and Capped Via Protection Material	1
Figure 3-1 Example of Hole Fill/Plug Separation from Plated Hole Wall	3
Figure 3-2 Example of Depression Within Fill/Plug Material	3
Figure 3-3 Voids in Via Fill Material	3
Figure 3-4 Large Voids in Via Fill Material	3
Figure 3-5 Corroding of Hole Wall Plating Resulting from Single-Side Via Protection	4
Figure 5-1 Examples of Type I Tented Vias	6
Figure 5-2 Examples of Type II Tented and Covered Vias	7
Figure 5-3 Examples of Type III Plugged Vias	8
Figure 5-4 Examples of Type IV Plugged and Covered Vias	8
Figure 5-5 Example of Type V Filled Via	9
Figure 5-6 Examples of Type VI Filled and Covered Vias, Dry Film Cover	9
Figure 5-7 Examples of Type VI Filled and Covered Vias, Liquid Film Cover	9
Figure 5-8 Examples of Type VII Filled and Capped Via	10
Figure 5-9 Examples of Partially Filled Vias	10
Figure 7-1 Illustration of "Tented and Covered" Via Protection Method	11
Figure 7-2 Design Rule formula with exploded view of tent and cover detail	11
Figure 7-3 Top View Illustration of Solder Mask Clearance around a BGA Pad	12
Figure 7-4 Top View Illustration of Overlap Detail for Tent and Covered Vias	12

Tables

Table 5-1 Application Guidelines for Via Protection Types	6
---	---

Design Guide for Protection of Printed Board Via Structures

1 SCOPE

The protection of through vias within Printed Wiring Boards (PWB) has evolved from limited use to common practice. Technology has evolved where via fabrication techniques and protection methodologies need to be defined to allow current designs to be manufacturable at an acceptable yield and cost. Numerous techniques and objectives exist, and will be discussed in this document. This document is the product of the IPC D-33d Via Protection Task Group and has been developed to provide guidance for the designer and fabricator on how via protection should be approached as well as guidance on how via protection should be specified in procurement documentation.

1.1 Purpose This guideline provides PWB designers, fabricators and/or users with information on existing methods for the protection of vias on printed boards. In addition to detailing some of the advantages of via protection, production and material issues are given to aid the user in evaluating the benefits and concerns for each type of protection.

1.2 Terms and Definitions The definition of all terms used herein shall be as specified in IPC-T-50 and as defined below.

Bumped Via Protection – Via protection where the hole plugging or fill material protrudes above the surface of the hole interface producing a convex shape. See Figure 1-1.

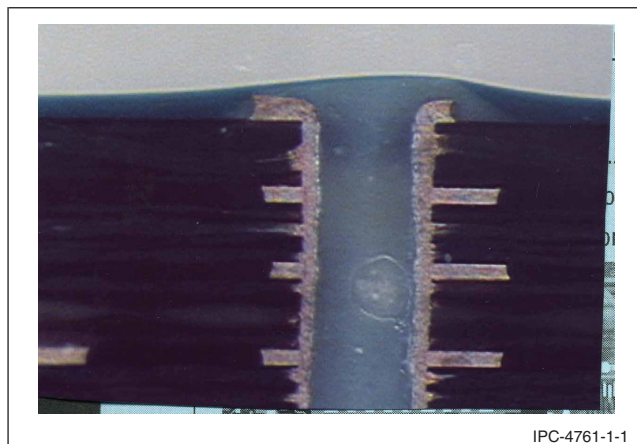


Figure 1-1 Bumped Via Protection Material

Dimpled Via Protection – Via protection where the hole plugging or fill material recedes below the hole interface producing a concave shape. See Figure 1-2.

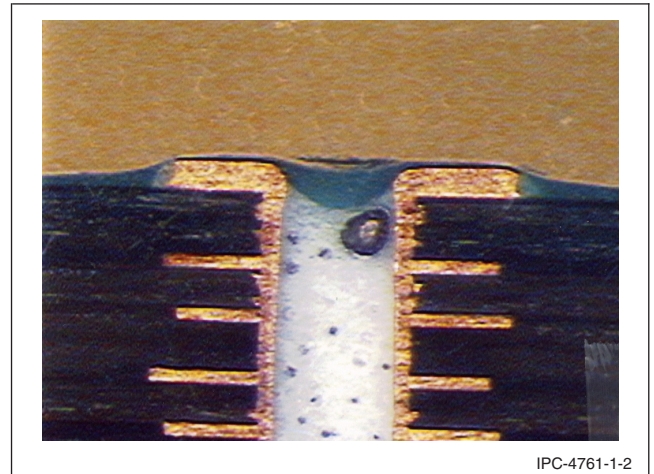


Figure 1-2 Dimpled Via Protection Material

Planarized Via Protection – Via protection where the excess hole plugging or fill material protruding above the hole interface has been removed by a process to produce a coplanar surface. See Figure 1-3.

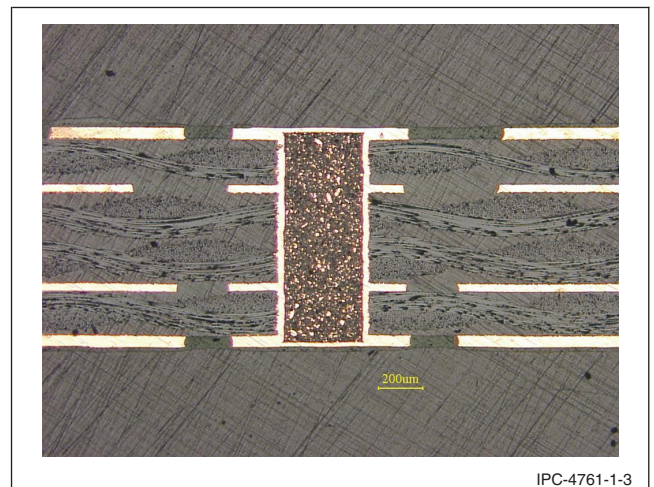


Figure 1-3 Planarized and Capped Via Protection Material

2 APPLICABLE DOCUMENTS

2.1 IPC¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-A-600 Acceptability of Printed Boards

IPC-SM-840 Qualification and Performance of Permanent Solder Mask

¹www.ipc.org