

IPC/JPCA-2291



Design Guideline for Printed Electronics



Developed by the Printed Electronics Design Subcommittee (D-61) of the Printed Electronics Committee (D-60) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC 3000 Lakeside Drive, Suite 309S Bannockburn, Illinois 60015-1249 Tel 847 615.7100 Fax 847 615.7105 JUNE 2013 IFO/JFOA-2291

Table of Contents

1 SCOPE			4 DESIGN PROCESS FLOW5		
1.1	Purpose	1	4.1 Printed	d Electronics Design Process Flow Stages 5	
1.2	Intent	1	4.1.1 Functi	on and Purpose Definition	
1.3	Printed Electronics Document Hierarchy	1	4.1.2 Perfor	mance Specifications	
1.4	Qualification	2	4.1.3 Materi	ials Selections	
1.5	Procurement Documentation	2	4.1.4 Design	and Architecture	
1.6	As Agreed Upon Between User and Supplier (AABUS)	2	_	facturing Process Layout	
1.7	Interpretation		4.1.6 Cost A	Analysis 20	
1.7	Presentation		4.1.7 Final l	Device, Module and Unit, and Product 21	
	PPLICABLE DOCUMENTS	2	5 NOTES .		
2.1	IPC		5.1 Data (Conversion Initiative Background	
2.2	NCSL International		6 REFEREI	NCES 23	
2.3	ISO	2		Figures	
3 TI	ERMS AND DEFINITIONS	3	Figure 1-1	Hierarchy for IPC/JPCA Printed	
3.1	base material*	3	ga	Electronics Documents	
3.2	barrier	3	Figure 1-2	Future Hierarchy for IPC/JPCA Printed Electronics Documents	
3.3	fiducial mark	3	Figure 4-1		
3.4	functional biologically active material	3	Figure 4-1	Printed Electronics Design Process Flow 8 Base Materials Family Designation	
3.5	functional chemically active material	3	Figure 4-2	Single Layer – Single-Sided Topology	
3.6	functional conductive material	3	Figure 4-3a	Single Layer – Single-Sided Topology	
3.7	functional dielectric material	3	Figure 4-3b	Single Layer – Single-Sided hith Printed	
3.8	functional material	3	i iguie 4-4a	Jumpers Topology	
3.9	functional optically active material		Figure 4-4b	Single Layer – Single-Sided with Printed Jumpers Topology	
3.10	functional semiconductive material		Figure 4-5a	Single Layer – Double-Sided Topology 1	
3.11	functional thermally active material		Figure 4-5b	Single Layer – Double-Sided Topology 1	
3.12	hybrid structure		Figure 4-6a	Multiple Layer – Single-Sided Topology 12	
3.13	in-body		Figure 4-6b	Multiple Layer – Single-Sided Topology 12	
3.14	nonfunctional material		Figure 4-7a	Multiple Layer – Double-Sided Topology 14	
3.15	nonprinted conductor		Figure 4-7b	Multiple Layer – Double-Sided Topology 14	
3.16	on-body		Figure 4-75	Definitions of Printed Layer and Feature	
3.17	printed electronics based devices	4	rigure 4-6	Attributes	
3.18	printed electronics based material		Figure 4-9a	Hybrid Single Layer – Single-Sided	
3.19	printed electronics based process			Topology	
3.20	printed electronics based final products		Figure 4-9b	Hybrid Single Layer – Single-Sided Topology17	
3.21	printed electronics based modules and units		Figure 4-10a	Hybrid Multiple Layer – Single-Sided	
3.22	printed electronics through-hole		119010 + 100	Topology	
3.23 3.24	printed electronics via		Figure 4-10b	Hybrid Multiple Layer – Single-Sided Topology17	
J.4 †	Surface IIIIISII	¬		10p010gy1	

This is a preview of "IPC/JPCA 2291-2013". Click here to purchase the full version from the ANSI store.

TFO/JFOA-2291 Julie 2013

Figure 4-11	Hybrid Structure – Printed Component with Nonprinted Microelectronics Topology
Figure 4-12	Example Printed Electronics Manufacturing Process Layout
Figure 4-13	Design Data Conversion Flow
Figure 4-14	Design Data Verification Flow
	Tables
Table 4-1	Printed Electronics – Design for Purpose
Table 4-2	Performance Specifications
Table 4-3	Printed Electronics Materials
Table 4-4	Single Layer - Single-Sided Design
Table 4-5	Single Layer – Single-Sided with Jumper Design10
Table 4-6	Single Layer - Double-Sided Design 1
Table 4-7	Multiple Layer - Single-Sided Design 13
Table 4-8	Multiple Layer – Double-Sided Design 19
Table 4-9	Interfaces and Interconnects 15
Table 4-10	Single Layer – Single-Sided Hybrid Structure Design1
Table 4-11	Multiple Layer – Single-Sided Hybrid Structure Design 18
Table 4-12	Manufacturing Process Layout Parameters 18
Table 4-13	Processing Technologies and Testing Parameters19
Table 4-14	Cost Analysis Parameters 20
Table 4-15	Design Data to Fabricate Printed

JUNE 2010 IFO/JFOA-2291

DESIGN GUIDELINES FOR PRINTED ELECTRONICS

1 SCOPE

This guideline provides an overview of the design process flow for printed electronics based devices, modules and units, and final products.

- **1.1 Purpose** The purpose is to present the framework of the design process flow for individuals to manufacture printed electronics based devices, modules and units, and final products.
- **1.2 Intent** The intent of IPC/JPCA-2291 is to establish a design process flow that will facilitate and improve the practice of printed electronics design. IPC/JPCA-2291 identifies documents such as standards that can be used to assist during the design process flow. In general IPC/JPCA-2291 contains generic information that is sufficient for printed electronics design by the product designer.

The subcommittee members that developed IPC/JPCA-2291 acknowledge that individual companies may require additional information than that reported within this document. Therefore, IPC/JPCA-2291 and documents specified within it may only reflect a subset of those required by members of the supply chain.

IPC/JPCA-2291 is "generic" because it specifies only information which forms the basis for further specific declarations. It is therefore intended to be used in conjunction with other documents as needed. Also, part of the intent is to provide mechanisms for securing the integrity of the information exchanged between supply chain members.

1.3 Printed Electronics Document Hierarchy The IPC/JPCA printed electronics standards development subcommittees have established a hierarchy as presented in Figure 1-1 based on the existing initiatives. It was structured to enable the greatest flexibility for the emerging field of printed electronics. The subcommittees plan to revisit it frequently and modify it as necessary during the growth of the field and technologies transition from R&D to commercialization.

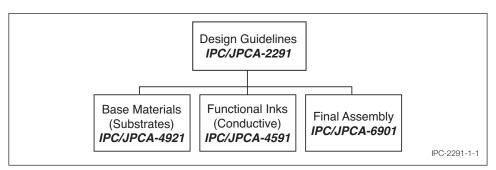


Figure 1-1 Hierarchy for IPC/JPCA Printed Electronics Documents

As the documents listed in Figure 1-1 are completed, new standards projects may be undertaken by the subcommittees. Proposed projects will be listed as shown in Figure 1-2; a project was proposed that addresses manufacturing processes and platforms. In addition to initiating new project topics, subcommittees may also be actively preparing a revision of a previously approved standard based on recent subcommittee member comments as well as general industry trends.

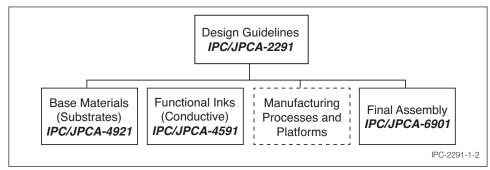


Figure 1-2 Future Hierarchy for IPC/JPCA Printed Electronics Documents