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IPC-7091

Design and Assembly Process Implementation of 3D Components

Developed by the 3-D Electronic Packages Subcommittee (B-11) of the Packaged Electronic Components Committee (B-10) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

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Design and Assembly Process Implementation of 3D Components

1 SCOPE

This document describes the design and assembly challenges and ways to address those challenges for implementing 3D component technology. Recognizing the effects of combining multiple uncased semiconductor die elements in a single-package format can impact individual component characteristics and can dictate suitable assembly methodology. The information contained in this standard focuses on achieving optimum functionality, process assessment, end-product reliability and repair issues associated with 3D semiconductor package assembly and processing.

1.1 Purpose Performance-driven electronic systems continue to challenge companies in search of more innovative semiconductor package methodologies. The key market driver for semiconductor package technology is to provide greater functionality and improved performance without increasing package size. The package interposer is the key enabler. Although glass-reinforced epoxy-based materials and high-density copper interconnect capability will continue to have a primary role for array-configured packaging, there is a trend toward alternative dielectric platforms as well as toward combining multiple functions within the same die element. To address this movement, an increasing number of semiconductor die developed for advanced applications now require higher I/O with contact pitch variations that are significantly smaller than the mainstream semiconductor products previously in the market. For these applications, companies are developing interposer technologies that can provide interconnect densities far superior to organic-based counterparts.

1.2 Target Audience The target audiences for this standard are managers, design/process engineers and operators who deal with:

- Implementing 3D semiconductor packaging
- Interposer, substrate and PWB design
- Board-level assembly, inspection and repair processes

1.3 Intent This standard intends to provide useful and practical information to those who are designing, developing or using 3D-packaged semiconductor components or those who are considering 3D package implementation. The 3D semiconductor package may include multiple die elements—some homogeneous and some heterogeneous. The package may also include several discrete passive SMT devices, some of which are surface mounted and some of which are integrated (embedded) within the components' substrate structure.

1.4 Definition of Requirements The imperative form of action verbs is used throughout this document to identify acceptance requirements that may require compliance, depending upon the Performance Classification of the hardware (see 12.3). To assist the User, these action verbs are in bold text.

a) The words **shall/shall not** are used whenever a requirement is intended to express a provision that is mandatory. Deviation from a **shall** or **shall not** requirement for a particular Performance Class may be considered if sufficient technical rationale/objective evidence (OE) is supplied to the User to justify the exception.

b) The word **should** is used whenever a requirement is intended to express a provision that is nonmandatory and which reflects general industry practice and/or procedure.

1.5 Implementation Challenges The next generation of 3D assembly has many implementation challenges, since the technology is complex and requires process expertise that may require foundries, outsourced semiconductor assembly and test (OSAT) providers and original design manufacturers (ODMs). There is no clear direction where 3D packages will be built, tested and assembled. The type of process to be used and the order of assembly and stacking is not defined and depends on the assembler's expertise.