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Troubleshooting for PBC Fabrication Processes

Amendment 1

Developed by the Printed Board Process Effects Handbook Subcommittee (7-24) of the Process Control Management Committee (7-20) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

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IPC

Table of Contents

Troubleshooting for PCB Fabrication Processes
Amendment 1

New Via Fill Section for Section 7 Hole Preparation and Protection

7.13 Via Fill The continued fast pace toward miniaturization is leading printed board designers to advance integration density. Because of this trend, fabricators are investigating methods and processes that will enable the move toward sequential lamination, blind and buried vias and via-in-pad technology. Many printed board fabricators are adopting techniques such as via filling capability with nonconductive, high-T_g, low-CTE plugging pastes.

Partially plugging some or all via holes with solder mask prevents solder from wicking through the holes (to the component side) during the assembly process creates a vacuum for electrical test and can minimize flux residues in the holes.

There are concerns with plugging through-holes with a standard liquid photoimageable (LPI) solder mask because these inks are typically 60% to 80% solids content. During the drying/curing process, the solvent evaporates and the hole plug shrinks, often resulting in a small gap between the through-hole barrel and the plug. This can result in a lack of adhesion of the plug to the hole wall. Another concern is residual solvents from the LPI. During the curing process, operating conditions may lead to a ‘‘skinning over’’ of the plug. This scenario causes solvent to remain entrapped within the hole. As a result, the solvent will expand during the heat of the soldering operations, leading to cracking of the fill. As through-hole aspect ratios increase, it may become impossible to evacuate all the solvent. Operators must carefully monitor process curing temperatures and ramp-up time to cure, regardless of the technology level of the printed board.

LPIs have limitations that can only be addressed with the use of plugging pastes. These plugging pastes are nearly 100% solids content and were primarily developed for blind and buried vias and sequential build technology. However, other formulations have been developed for filling through-holes to replace LPI inks, based on the same principle of 100% solids content.

Via hole filling is used for nonplanar filling of plated through-holes. Via hole plugging is the planarization of blind vias, buried vias and through-holes. Via hole plugging is applicable to HDI and microvia designs. Brushing (or planarization) is required to remove the excess material and to create the flat surface.

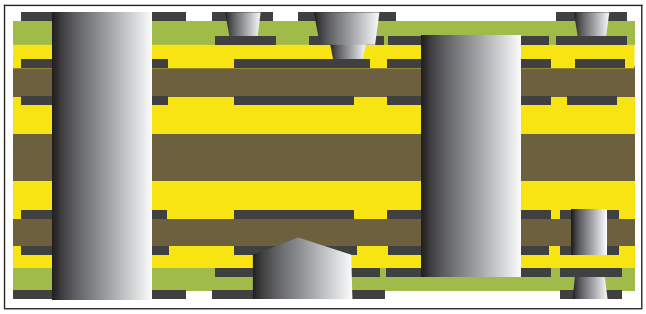

Figure 7.13-1 HDI Substrate With Plugged Vias

Via hole plugging is in demand due to HDI designs with area array for IC packaging, via-in-pad and landless designs as well as to achieve planarity of the via for dielectric formation. Uniform dielectric spacing between layers of circuitry is critical, as is the ability to metallize the dielectric to achieve plating adhesion.

Figure 7.13-1 shows an HDI substrate with plated through-holes, filled buried vias and microvias. In this example, all the via types would be candidates for filling.

The vias can be described as follows:

- Completely plugged and over-metallized via-in-pad
- Completely plugged buried vias over several layers as necessary
- Completely plugged and over-metallized buried vias over several layers as necessary

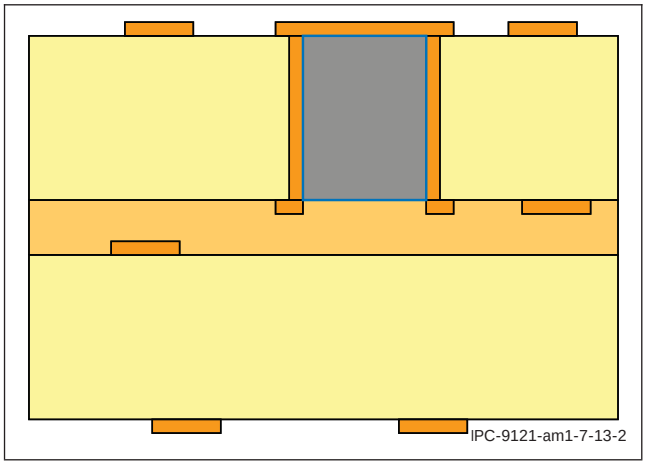

Figure 7.13-2 Over-Metallized Via-in-Pad

One of the most widely used applications for plugging paste is for via-in-pad designs (see Figure 7.13-2).

Several OEMs are driving the industry to migrate to high-T_g/low-CTE plugging paste formulations for high-density applications. These formulations are of a nonconductive nature, which provides a high-quality plugged via, and they are cost-effective.